CIRCUIT AND METHOD FOR GENERATING FIXED POINT DATA WITH REDUCED CIRCUIT SCALE

Abstract of the Disclosure

A decoding rate is improved while reducing a circuit scale, in a fixed point data generating circuit. When a plurality of floating point data are inputted, for example, the maximum floating point data is detected as a reference data among the plurality of floating point data, in a MAX value detecting circuit 10. Then, in an exponent part subtractor 20, differences are obtained between the values of exponent parts of the plurality of inputted floating point data and the value of an exponent part of the maximum floating point data. Thereafter, in the shift register 30, mantissa parts of the inputted floating point data are shifted by the differences obtained in the exponent part subtractor 20, and, in a bit extracting portion 40, a predetermined number of bits of the shifted mantissa parts are extracted as fixed point data to be inputted to a Viterbi decoder.